

Development of Nanomaterial-Based Physically Unclonable Functions and Dedicated Measurement and Testing Devices

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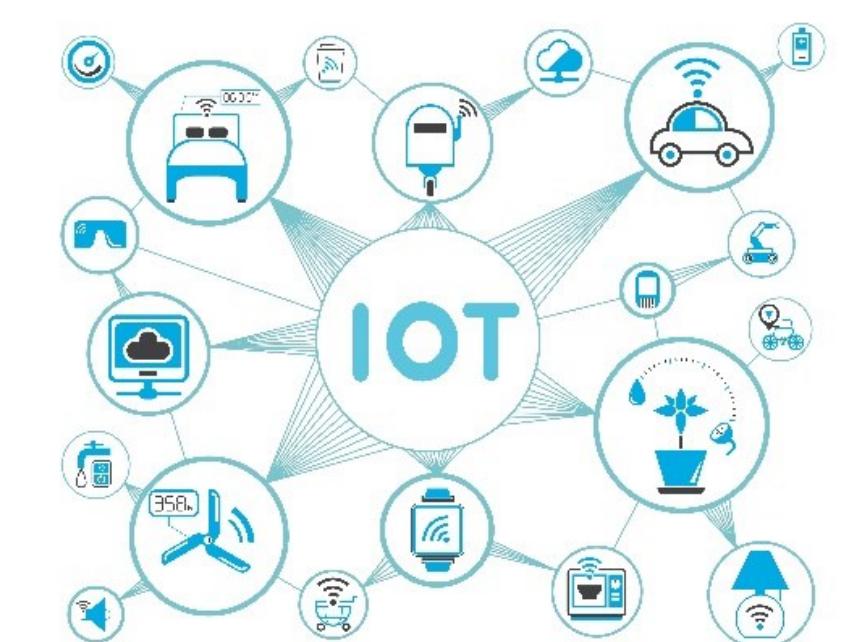
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Introduction and Motivation

Progressive digitalization of connected cyber-physical systems in recent years accelerated by...

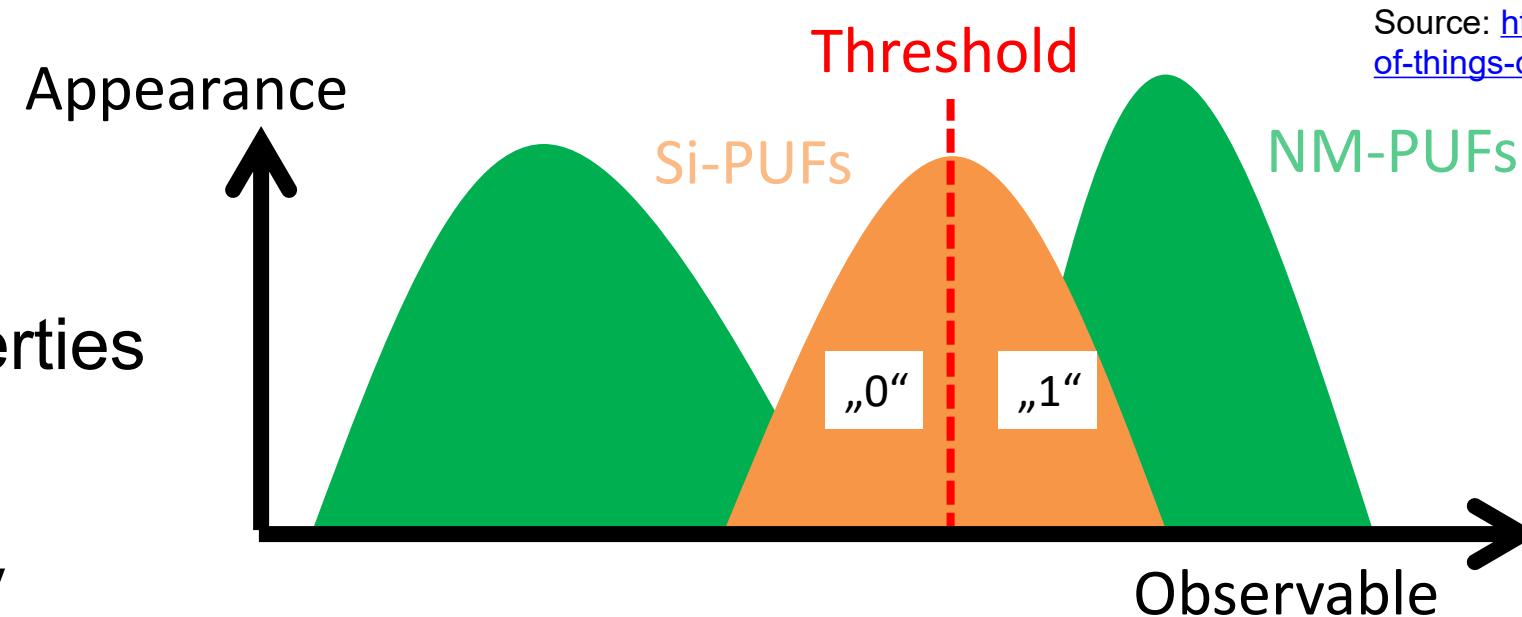
- Autonomous driving – Trustworthy sensor data?
- Internet of things – Privacy?
- 5G / 6G / Edge computing – Secure communication?

- High demand for embedded hardware security solutions – **Physical Unclonable Functions (PUFs)**



Unique selling points for nanomaterial PUFs (NM-PUFs)

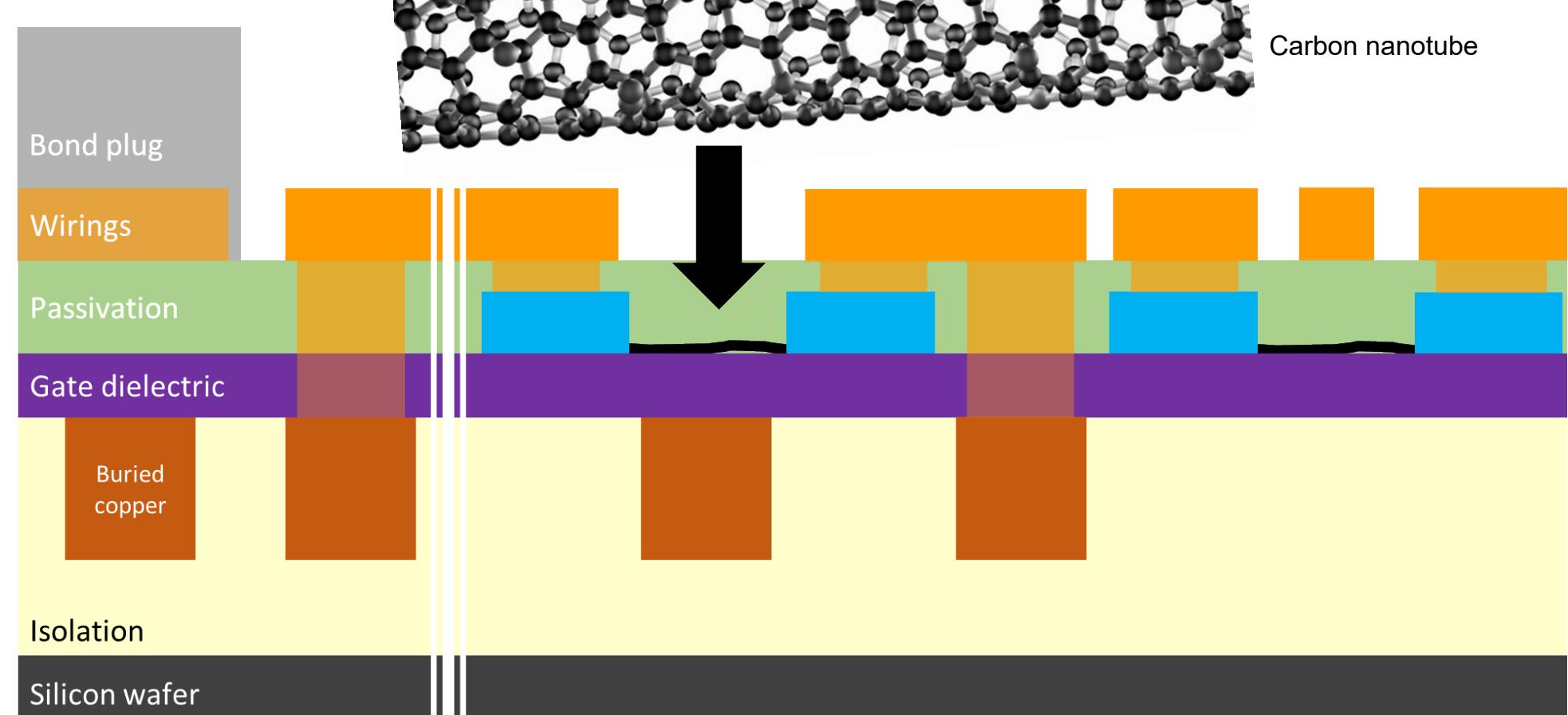
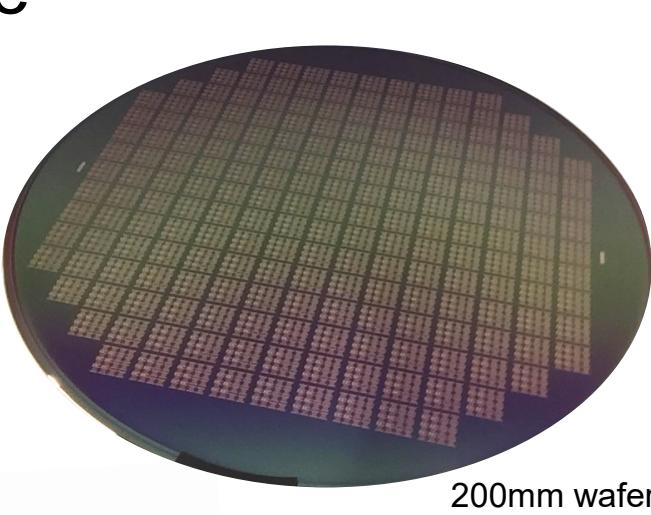
- Miniaturization
- Multi-bit keys – multi-entropy sources
- High key robustness – non-normal distributed NM-FET properties
- High tamper-evidence – surface-only nanomaterial
- Multifunctional – CNT-FET for electronics, sensors & security



CNT Transistor Fabrication

CMOS-compatible 200mm nanodevice technology platform (TU Chemnitz)

Systematic variation of process parameters & device geometry for highest entropy of ternary bit PUFs

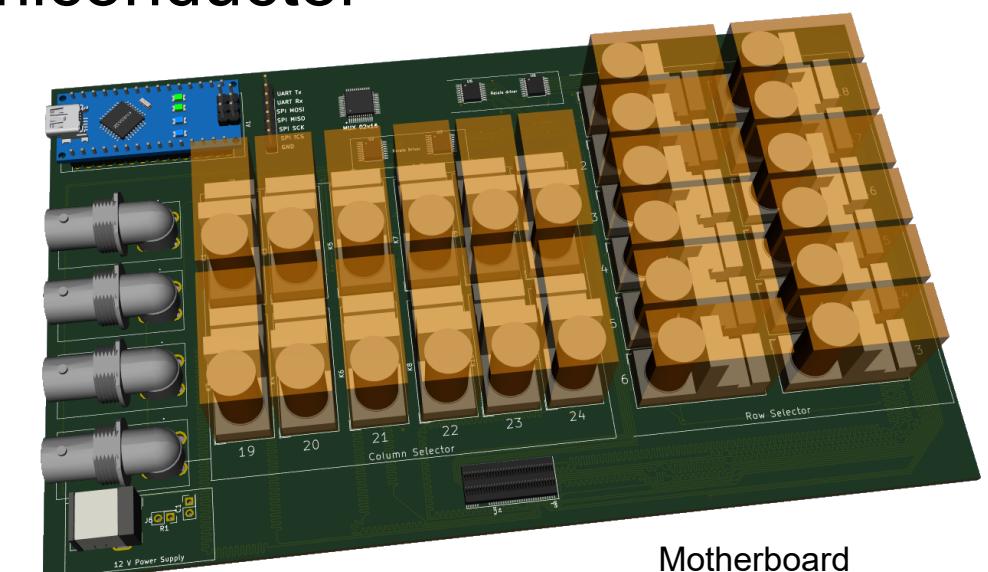
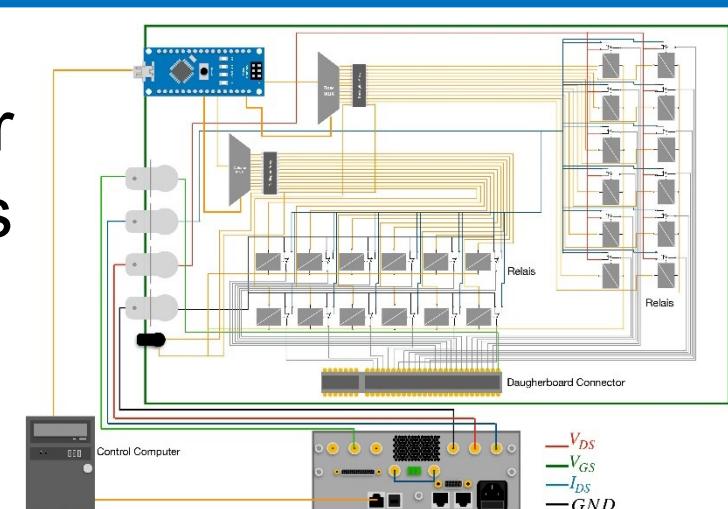


Measurement and Testing Setup

Construction of adequate test setup for systematical and statistical investigations (University of Passau)

Mother- / Daughterboard configuration:

- NM-PUF mounted and wire-bonded on daughterboard
- Readout switch matrix on motherboard with connectors to a Source Measurement Unit (SMU), which acts as a semiconductor parameter analyzer

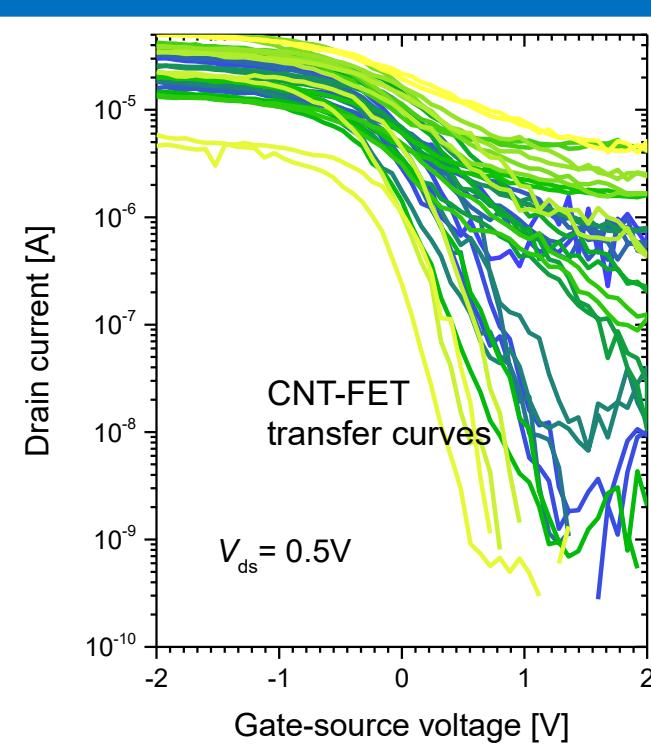
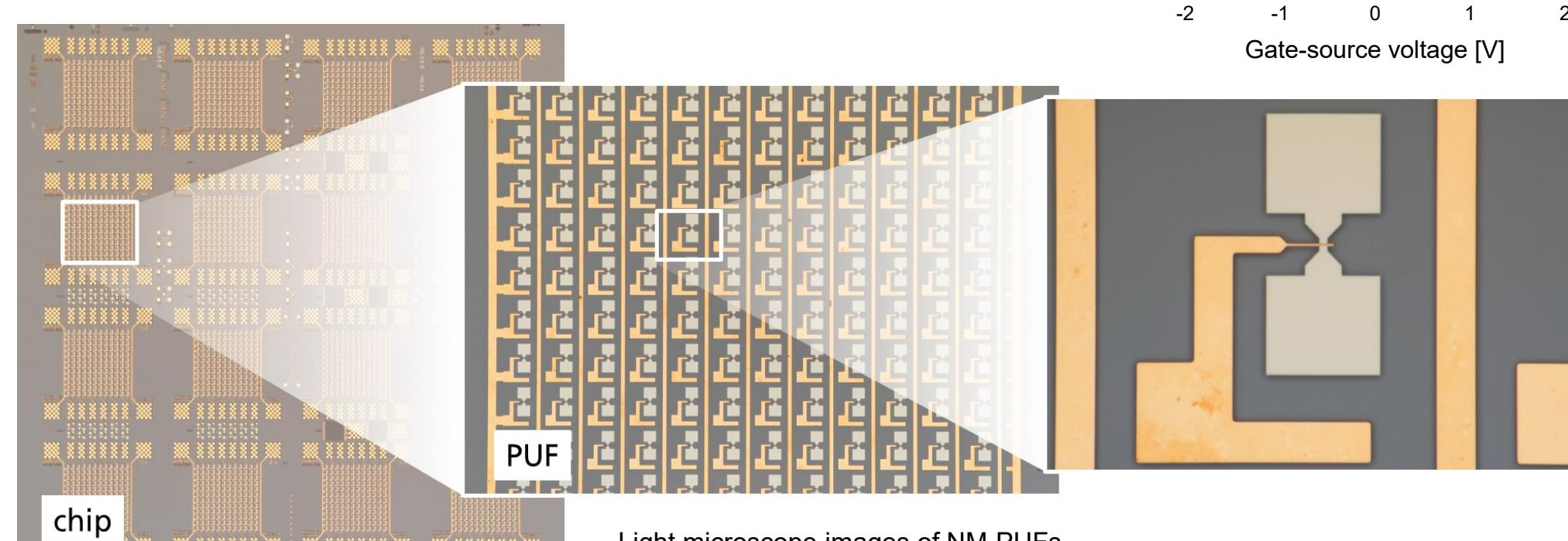


Results

Fabrication of 144-bit NM-PUFs based on CNT-FET arrays on 200mm silicon wafers

CNT integration method

- Printing approach with water- or solvent-based inks (CNT dispersions)



Automatic I-V scanning of more than 8000 sites per wafer @ $V_{DS} = 0.1$ V



Distribution of open circuit ("0") and closed circuit ("1") strongly depends on width of transistor channel

Systematic study:

- Revealing binary and ternary NM-PUFs with the highest entropy

